criticisms in the Official Action, to place the application in condition for allowance at the time of the next Official Action.

Claims 1 and 13 have been canceled and claims 23-25 have been added, leaving claims 2-12, and 23-25 in the application.

Claims 1-3 were rejected as unpatentable over the admitted prior art (APA) in view of DIODATO et al. US2002/0079522 A1. Claim 1 has been canceled and claims 2-3 have been amended to depend from claim 6. Reconsideration and withdrawal of the rejection are respectfully requested.

Claims 6-9 were rejected as unpatentable over the APA in view of DIODATO et al. and PAREKH et al. US2002/0058380 A1. Reconsideration and withdrawal of the rejection are respectfully requested.

Among other features, claim 6 provides that the second contact through the first inter-level dielectric includes a second metal portion formed of the same metal as the metal that forms the first contact. The Official Action relies on PAREKH et al. for the suggestion to provide the second contact, without mentioning that the second contact is to be formed of the same metal as the first contact. PAREKH et al. suggest that the contacts therein are polysilicon (paragraph 0025). There is nothing in the combination that suggests to one of skill in the art that the same metal be used to form both the first and second contacts. Accordingly, it is believed that claim 6 and claims 2-

5 and 7-9 dependent therefrom are allowable over the suggested combination.

New claim 23 provides, among other features, that the first and second contacts and the bit line contact plug are all formed of a same first metal. There is no suggestion in the references to make all three of these elements the same metal and thus the new claims are believed to avoid the rejections of record.

Claims 4-5 and 10-11 were rejected as unpatentable over APA in view of DIODATO et al., and AMICO et al. US2001/0014498 A1. Claims 4-5 and 10-11 depend from claim 6 and are allowable for reasons given above.

Claim 12 was rejected as unpatentable over the APA in view of DIODATO et al., AMICO et al. and FUKUDA et al. US2002/0079526 A1. Claim 12 depends from claim 6 and is allowable for the reasons given above.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

Attached hereto is a marked-up version showing the changes made to the specification and claims. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

Respectfully submitted,

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"VERSION WITH MARKINGS TO SHOW CHANGES MADE"

IN THE SPECIFICATION:

Page 20, the paragraph, beginning on line 25, bridging pages 20 and 21, has been amended as follows:

--As shown in Fig. 2, the inter-level dielectric 16 is covered with a silicon [oxinitride] oxynitride film 21 and an inter-level dielectric 22. The inter-level dielectric 22 is formed of silicon oxide deposited by a plasma CVD (chemical vapor deposition) method. The silicon [oxinitride] oxynitride film 21 is an etching stopper for etching of the inter-level dielectric 22.--.

IN THE CLAIMS:

Claim 2 has been amended as follows:

--2. (amended) The semiconductor memory device according to claim [1] 6, wherein said metal is a refractory metal, and said first contact further includes a barrier layer formed between said source and said first metal portion.--

Claim 3 has been amended as follows:

--3. (amended) The semiconductor memory device according to claim 2, wherein said refractory metal is tungsten, and said [contact] barrier layer is formed of titanium nitride.--

Claim 6 has been amended as follows:

--6. (amended) [The semiconductor memory device according to claim 1, further comprising:] A semiconductor memory device comprising:

a substrate;

a MOS (metal oxide semiconductor) transistor formed in a surface portion of said substrate, wherein said MOS transistor includes a source, a gate, and a drain;

a first inter-level dielectric covering said MOS transistor;

a capacitor element including:

a bottom electrode,

a dielectric layer formed on said bottom electrode, and

an upper electrode formed on said dielectric layer;

a first contact formed through said first inter-level dielectric to electrically connect said bottom electrode to said source, wherein said first contact includes a first metal portion formed of metal; and

a second contact formed through said first inter-level dielectric to be connected to said drain, wherein said second contact includes a second metal portion formed of said metal.--

Claim 10 has been amended as follows:

--10. (amended) The semiconductor memory device according to claim [1] 6, wherein said bottom electrode comprises:

a polysilicon layer connected to said dielectric layer, and

an electrode barrier layer formed between said first metal portion and said polysilicon layer.--